PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Raymond Li
Docket No: 0100.01142
Title: METHOD AND APPARATUS OF VIDEO GRAPHICS AND AUDIO PROCESSING

To the Honorable Commissioner
of Patents and Trademarks
Box Patent Application
Washington, D.C. 20231

Date: March 20, 1998

TRANSMITTAL LETTER FOR FILING A NATIONAL PATENT APPLICATION

The applicant hereby respectfully requests that the above captioned patent application be accepted for examination. This patent application is a:

- ☒ new patent application;
- ☐ continuation in part (CIP) of Application Serial No. filed on ;
- ☐ divisional application of Application Serial No. filed on ;
- ☐ continuation of Application Serial No. filed on ;

Accompanying this request is (as indicated by an "X" in the corresponding box):

☒ 1. 17 pages of specification, which includes the claims and abstract, and 4 sheets of formal drawings;

☒ 2. Combined Declaration and Power of Attorney;

☐ 3. An Information Disclosure Statement along with the references;

☐ 4. A petition to extend the response for a priority application identified above;

☒ 5. An assignment assigning all rights in the above referenced patent application to ATI Technologies, Inc.;

☒ 6. An assignment recording cover sheet;

☐ 7. A verified statement establishing small entity status under 37 C.F.R. Sections 1.9 and 1.27;

☒ 8. A certificate of mailing indicating that the above captioned patent application has been deposited as "Express Mail" with the United States Postal Service;

☐ 9. A certificate of mailing indicating that the above captioned patent application has been deposited with the United States Postal Service with sufficient postage as first class mail;

☒ 10. A return postcard; and

☐ 11. A preliminary amendment.

The filing fee for the above captioned patent application is as follows:

	Data Entry	
Basic filing fee	xxxxx	$ 790 00
Total No. of Claims	23	$ 66.00
Total No of Ind Claims	4	$ 82 00
Assignment Recording Fee	xxxxx	$ 40.00
Total Filing Fee		$ 978.00

Payment of the above calculated filing fee is as follows (as indicated by the "X" in the corresponding box):

☐ A check in the amount of $;

☒ Please charge Deposit Account No. 50-0441 in the amount of $978.00. A duplicate sheet is attached. The Commissioner is hereby authorized to charge or credit any additional amounts regarding this patent application to the same Deposit Account.

Respectfully submitted,

By: _____

Timothy W. Markison
Registration No: 33,534
Phone: (972) 547-6477
Fax: (972) 547-1144

Please send all correspondence to:
Markison & Reckamp, P.C.
P.O. Box 677
Northbrook, IL 60065

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Raymond Li | Examiner:
Serial No: | Art Group:
Filing Date: | Docket No: 0100.01142
Title: METHOD AND APPARATUS OF VIDEO GRAPHICS AND AUDIO PROCESSING

To the Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF EXPRESS MAILING

Express Mail Label No: EI904617376US Name of Depositor: TIM MARKISON (print or type)

Date of Deposit: MARCH 24, 98 Signature: Tim Mark

I hereby certify that this paper and the items identified below are being deposited with the U.S. Postal Service "Express Mail Post Office to Addresses" service under 37 C.F.R. Section 1.10 on the 'Date of Deposit', indicated above, and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Items accompanying this Certificate of Express Mailing:

☒ Filing papers for a new patent application or PCT application entitled invented by and having a docket no. of , such filing papers include:

- ☒ A specification and drawings for a new patent application;
- ☒ Transmittal cover letter;
- ☒ Assignment agreement;
- ☒ Assignment Cover Sheet;
- ☒ Combined Declaration and Power of Attorney;
- ☐ Statement of Small Entity Status;
- ☐ Information Disclosure Statement;
- ☒ Return upon receipt post card;

☐ Filing of a correspondence in an interference which an examiner-in-chief ordered to be filed by hand or "Express Mail";

☐ Filing of an agreement between parties to an interference under 35 U.S.C. 135 (c);

☐ Filing of correspondence in an international application before the U.S. Receiving Office, the U.S. International Searching Authority, or the U.S. International Preliminary Examining Authority;

☐ Filing of a copy of the international application and the basic national fee necessary to enter the national stage, as specified in 37 C.F.R. Section 1.494 (b) or 37 C.F.R. Section 1.495(b).

PATENT APPLICATION

0100.01142

METHOD AND APPARATUS OF VIDEO GRAPHICS AND AUDIO PROCESSING

Technical Field of the Invention

This invention relates generally to computer peripherals and more particularly to graphics processing and audio processing.

Background of the Invention

Computers are known to include a central processing unit ("CPU"), main memory, system buses, and a plurality of supporting units. Such supporting units include audio processing circuitry, video processing circuitry, graphical user interface modules, etc. Physically, many of the supporting units are mounted or coupled to a motherboard. Each of the supporting units, when coupled to the motherboard, includes a local bus that couples the supporting unit to the system bus.

In operation, when the CPU is inputting, or outputting, data from a supporting unit, it generates an address and a command, which are provided on the system bus. Each of the supporting units, via its local bus, monitors the address bus to determine whether the particular command is directed to it. When the appropriate supporting unit detects that the command is for it, it performs the command. If the command is to input data, the supporting unit stores, and processes –if instructed-, the data provided by the CPU. If the

command is to output data, the supporting unit outputs the data via the local bus to the system bus and routes it either to the CPU, or a designated recipient.

In a typical computer, the video graphics processing circuitry is on a separate board than the audio processing circuitry. As such, the video graphics circuit board and the audio processing circuit board each have their own local buses. In addition, they each require coupling to the motherboard and function as totally independent circuits. A typical audio processing circuit board will retail for approximately $30.00, which, in turn, relates to approximately $15.00 of manufacturing costs. With the ever-increasing demand for smaller, more powerful, and less expensive computers, it would be desirable to reduce the cost of including an audio processing circuit.

Therefore, a need exists for a method and apparatus of a graphics circuit and audio processing circuit contained on a single chip and/or printed circuit board.

Brief Description of the Drawing

Figure 1 illustrates a schematic block diagram of a computer system in accordance with the present invention;

Figure 2 illustrates a schematic block diagram of the bus arbitration circuit of Figure 1;

Figure 3 illustrates a schematic block diagram of a video graphics and audio processing circuit in accordance with the present invention;

Figure 4 illustrates a schematic block diagram of an arbitrator in accordance with the present invention; and

Figure 5 illustrates a logic diagram of a method for processing graphics and audio in accordance with the present invention.

Detailed Description of a Preferred Embodiment

Generally, the present invention provides a method and apparatus for combining video graphics processing and audio processing onto a single chip and/or the same printed circuit board. The combined circuit includes a graphics processing circuit, an audio processing circuit, a local bus, and a bus arbitrator. The local bus couples both the graphics processing circuit and audio processing circuit to the system bus such that each of the circuits may transceive data with the system bus. The bus arbitrator arbitrates access to the local bus between the graphics processing circuit and audio processing circuit. Such arbitration is based on incoming data, which is interpreted and, based on the interpretation, the bus arbitrator routes the incoming data to either the graphics processing circuit or the audio processing circuit. In addition, the bus arbitrator arbitrates outputting data from the graphics processing circuit and the audio processing circuit based on commands received from the CPU. With such a method and apparatus, a single local bus may be used for both the graphics processing circuit and audio processing circuit. By combining the audio processing circuit with the video graphics processing circuit, the costs of adding audio processing to a computer is substantially reduced, since the only cost incurred for adding audio is to include an audio codec and the bus arbitration circuit which is in the $2.00 to $3.00 range.

The present invention can be more fully described with reference to Figures 1 through 5. Figure 1 illustrates a schematic block diagram of a computer 10 that includes a CPU 12, a video graphics and audio processing circuit 14, and a system bus 16. The video graphics and audio processing circuit 14 includes a local bus 18, a bus arbitrator 20, an audio processing circuit 22, and a graphics processing circuit 24. The audio processing circuit 22 includes circuitry to process analog audio and digitized audio. Such circuitry

may include a wave table, audio playback circuitry, audio record, a mixer, and an audio codec. The video graphics processing circuit 24 includes circuitry to process analog video and digitized video signals. Such digitized video signals may be generated by the CPU based on software applications, such as a word processing document, graphics document, reading a CD drive. The analog video signals may come from a television encoder that is coupled to receive television broadcasts, cable broadcasts, satellite broadcasts, VCR transmissions and/or DVD transmissions. The video graphics circuit 24 may be equivalent to the video graphics circuit contained in the All-In-Wonder circuit manufactured and distributed by ATI Technologies.

In operation, the CPU generates commands for inputting and/or outputting data to/from the audio processing circuit and graphics processing circuit. Such commands include an address and an indication as to whether the command is for inputting data, outputting data, and/or processing data. The CPU places the command on the system bus, which is monitored by the bus arbitration circuit 20. When the bus arbitration circuit 20 recognizes the address for either the audio processing circuit 22 or the graphics processing circuit 24, it retrieves the command from the bus. The bus arbitration circuit 20, after interpreting the command, provides the command to either the audio processing circuit 22 or the graphics processing circuit 24. Such an interpretation is based on the address provided by the CPU.

The bus arbitration circuit 20 can be described in greater detail with reference to Figure 2. As shown, the bus arbitration circuit 20 includes an address decoder 30 and an output data switch 32, both of which are coupled to the audio processing circuit 22 and the graphics processing circuit 24. The address decoder 30 includes a data router 34 and control circuitry 36. The output data switch 32 includes a graphics buffer 38, an audio buffer 40, and a multiplexor 42.

The address decoder 30 is operably coupled to receive addresses 44 and data 46 via the local bus 18. The addresses 44 are provided to the data router 34 and the control circuitry 36. The data router 34 interprets the address 44 to determine whether the received data 46 is for the audio processing circuit 22 or the graphics processing circuit 24. Such an interpretation may be done by a look-up table or other equivalent address matching schemes. Based on the interpretation, the router 34 then acts as a switch to direct the received data 46 to the appropriate circuit 22 or 24.

The control circuitry 36 also interprets the address 44 to provide an enable/disable command signal 54 to the audio processing circuit and the graphics processing circuit 24. For incoming data, or received data 46, the control circuitry 36 generates an enable signal 54 to enable the appropriate circuit 22 or 24 to receive the data. The control circuitry 36 also receives a data command signal 48 from the CPU via the local bus 18. The data command may be a read command, write command, a read and write command, and/or a processing command.

If the data command signal 48 is a write command, the received data 46 is provided to the appropriate circuit 22 or 24 and stored therein. If the data command signal 48 is a read command, the control circuitry 36 provides an enable signal and a read command signal to the appropriate circuit 22 or 24. The appropriate circuit provides an output that is provided to the output data switch 32. In particular, the audio processing circuit 22 produces an audio output data 58, and the graphics processing circuit 24 produces graphics output data 56. If the data command signal 48 is a write-modified read command, the control circuitry provides such an indication via the enable/command signal 54 to the appropriate circuit 22 or 24. The appropriate circuit then writes the data, performs the requested modification, and then provides the data to the output data switch 32.

The output data switch 32 receives the graphics output data 56 into a graphics buffer 38. Similarly, the output data switch 32 receives the audio output data 58 in an audio buffer 40. The graphics buffer 38 and the audio buffer 40 may be first in/first out ("FIFO") buffers. The output of the buffers are provided to multiplexor 42 which is controlled via an output data control signal 50. The control circuitry 36 generates the output data control signal 50 based on the addresses 44 and the data command signals 48. Based on this control signal 50, the multiplexor 42 outputs data as data output 52.

When the data commands are for the audio processing circuit or the graphics processing circuit 24 only, the data output 52 will be either the graphics output data 56 or the audio output data 58. If, however, multiple data command signals 48 are addressed to both the audio processing circuit and the graphics processing circuit to generate a stream of data. the output data 52 will be graphics output data 56 intermixed with the audio output data 58. This is shown graphically as an intermixed data output signal 52. Thus, by including a bus arbitration circuit, the video graphics processing and audio processing may be combined onto a single chip and/or printed circuit board requiring only a single local bus interface to the system bus and single connector to interface with the mother board. By combining the audio processing and video graphics processing, the cost for including audio processing in a computer is substantially reduced.

Figure 3 illustrates a schematic block diagram of a video graphics and audio processing circuit 70. The processing circuit 70 includes memory 72 and a processing unit 74. The processing unit 74 may be a micro-processor, microcomputer, microcontroller, digital signal processor, CPU and/or any device which manipulates digital information based on programming instructions. The memory may be random access memory, read-only memory, magnetic tape memory, hard-drive memory, floppy disk memory, CD memory, DVD memory and/or any device that stores digital information.

The memory 72 stores programming instructions that, when read by the processing unit, causes the processing unit to function as a plurality of circuits 76-80. While reading the programming instructions, the processing unit functions as a circuit to receive at least one address and data command. The data command may be for inputting or outputting data from the processing circuit 70. The address will identify either audio processing or video processing. When a plurality of addresses are received, they may be for audio processing, video graphics processing or a combination thereof.

The processing unit 74 further executes programming instructions to function as circuit 78. As circuit 78, the processing unit audio processes the associated data command when the address identifies audio processing. The processing unit 74 also performs programming instructions that cause it to function as circuit 80. At circuit 80, the processing unit 74 graphic processes the associated data command when the address identifies graphic processing. The processing circuit 70 outputs the processed data, whether audio processed or graphics processed, to the system bus via a single local bus. As such, the audio and video graphics processing circuit may be implemented by a single processing unit or a plurality of processing units contained on a single chip and/or printed circuit board that includes a single local bus.

Figure 4 illustrates a schematic block diagram of an arbitrator 90. The arbitrator 90 includes memory 92 and a processing unit 94. The processing unit 94 may be a microcomputer, microprocessor, microcontroller, digital signal processor, central processing unit, digital logic control, and/or any other device that manipulates digital information based on programming instructions. The memory 92 may be read-only memory, random access memory, floppy disk memory, hard drive memory, magnetic tape memory, CD ROM memory, DVD memory, and/or any device that stores digital information.

The memory 92 stores programming instructions that, when read by the processing unit 94, causes the processing unit 94 to function as a plurality of circuits 96 and 98. While performing the programming instructions, the processing unit 94 functions as circuit 96. As circuit 96, the processing unit receives at least one address and determines whether the address identifies audio processing or graphics processing. The processing unit then functions as circuit 98 to arbitrate access to a local bus between an audio processing circuit and a graphics processing circuit. The programming instructions performed by the arbitrator 90 will be discussed in greater detail with reference to Figure 5.

Figure 5 illustrates a logic diagram of a method for arbitrating access to a local bus between a video graphics processing circuit and an audio processing circuit contained on the same single chip and/or printed circuit board. The process begins at step 100 where at least one address and an associated command is received. For each address received, there may be an associated command such that each request of the graphics and audio processing circuit is requesting a different action to be performed. For example, the associated command may be for inputting data (i.e., writing data), outputting data (i.e., reading data) or a write-modify read command.

The process then proceeds to step 102 where a determination is made as to whether the address or addresses identify the audio processing circuit or the graphics processing circuit. If the address or addresses only identify the audio processing circuit, the process proceeds to step 106. At step 106, the associated command is provided to the audio processing circuit and the audio processing circuit is provided with access to the local bus such that the processing of the command may be performed. If, however, the address or addresses only identify the video graphics processing circuit, the process proceeds to step 104. At step 104 the video graphics processing circuit is provided access to the local bus such that it may process the associated command or commands.

If, however, multiple addresses, or at least one, identify both the audio processing and graphics processing to produce a stream of data, the process proceeds to step 108. At step 108 access to the local bus is arbitrated between the audio processing circuit and the graphics processing circuit such that the respective circuits may perform the appropriate command. The arbitration will be based on the number of commands and/or the volume of data being processed by the appropriate circuits. As such, the video graphics circuit will have access to the local bus the majority of the time with the audio processing circuit being intermixed therewith. Such intermixing may be programmable to enhance performance of data throughput.

The preceding discussion has presented a method and apparatus for video graphics and audio processing being done on a single chip and/or printed circuit board. By integrating video graphics and audio processing onto a single chip and/or printed circuit board, the cost of adding audio processing into a computer is substantially reduced. As previously mentioned, the costs for a separate audio processing board is $30.00 retail and approximately $15.00 to manufacture. By integrating the audio processing onto the video graphics board, the cost is reduced to a few dollars of manufacturing cost.

Claims

What is claimed is:

1. A video graphics and audio processing circuit comprising:

a graphics processing circuit;

an audio processing circuit;

a local bus operably coupled to transceive data to and from the graphics processing circuit and the audio processing circuit; and

a bus arbitrator operably coupled to the local bus, the graphics processing circuit, and the audio processing circuit, wherein the bus arbitrator interprets incoming data and provides the incoming data to the audio graphics processing circuit or to the video graphics processing circuit, and wherein the bus arbitrator arbitrates outputting data on the bus from the graphics processing circuit and the audio processing circuit.

2. The video graphics and audio processing circuit of claim 1, wherein the bus arbitrator comprises an address decoder operably coupled to receive an address via the bus, to route received data to the audio processing circuit when the address identifies the audio processing circuit and to route received data to the graphics processing circuit when the address identifies the graphics processing circuit.

3. The video graphics and audio processing circuit of claim 2, wherein the address decoder comprises control circuitry that generates an output data control signal based on the address and a data command signal.

4. The video graphics and audio processing circuit of claim 3, wherein the bus arbitrator further comprises an output data switch operably coupled to output data to the bus from the audio processing circuit or the graphics processing circuit based on the output data control signal.

5. The video graphics and audio processing circuit of claim 4, wherein the output data switch comprises an audio buffer that stores audio output data generated by the audio processing circuit, an graphics buffer that stores graphics output data generated by the graphics processing circuit, and a multiplexor operably coupled to the audio buffer and the graphics buffer, wherein the multiplexor outputs the audio output data or the graphics output data based on the output data control signal.

6. A method for bus arbitration between an audio processing circuit and a graphics processing circuit. the method comprises the steps of:

a) receiving at least one address:

b) determining whether the at least one address identifies at least one of: the audio processing circuit and the graphics processing circuit; and

c) when the at last one address identifies both the audio processing circuit and the graphics processing circuit, arbitrating access to a local bus between the audio processing circuit and the graphics processing circuit.

7. The method of claim 6, wherein step (a) further comprises receiving an associated command for each of the at least one address.

8. The method of claim 7 further comprises enabling the audio processing circuit to receive incoming data via the local bus when at least one address identifies the audio processing circuit and when the associated command is for inputting data.

9. The method of claim 7 further comprises enabling the graphics processing circuit to receive incoming data via the local bus when at least one address identifies the graphics processing circuit and when the associated command is for inputting data.

10. The method of claim 7 further comprises providing the audio processing circuit access to the local bus when the at least one address identifies the audio processing circuit and the associated command is for outputting data.

11. The method of claim 7 further comprises providing the graphics processing circuit access to the local bus when the at least one address identifies the graphics processing circuit and the associated command is for outputting data.

12. The method of claim 7. wherein the at least one address comprises a plurality of addresses.

13. The method of claim 12 further comprises intermixing the audio processing circuit's access to the local bus with the graphics processing circuit's access to the local bus based on the plurality of addresses and the associated command.

14. A video graphics and audio processing circuit comprising:

a processing unit; and

memory operably coupled to the processing unit, wherein the memory stores programming instructions that, when read by the processing unit, cause the processing unit to receive at least one address and an associated data command for each of the at least one address; audio process the associated data command when the at least one address identifies audio processing, and graphics process the associated data comment when the at least one address identifies graphics processing.

15. The video graphics and audio processing circuit of claim 14, wherein the memory further comprises programming instructions that cause the processing unit to determine whether the associated data command is for inputting data or outputting data.

16. The video graphics and audio processing circuit of claim 15, wherein the memory further comprises programming instructions that cause the processing unit to intermix outputting audio data and graphics data when the at least one address includes a plurality of addresses that identify both the audio processing and graphics processing.

17. An arbitrator that arbitrates access to a local bus between graphics processing circuit and an audio processing, the arbitrator comprising:

a processing unit; and

memory operably coupled to the processing unit, wherein the memory stores programming instructions that, when read by the processing unit, cause the processing unit to receive at least one address, determine whether the at least one address identifies at least one of: the audio processing circuit and the graphics processing circuit; and arbitrate access to the local bus between the audio processing circuit and the graphics processing circuit when the at last one address identifies both the audio processing circuit and the graphics processing circuit.

18. The arbitrator of claim 17. wherein the memory further comprises programming instructions that cause the processing unit to receive an associated command for each of the at least one address.

19. The arbitrator of claim 18, wherein the memory further comprises programming instructions that cause the processing unit to enable the audio processing circuit to receive incoming data via the local bus when at least one address identifies the audio processing circuit and when the associated command is for inputting data.

20. The arbitrator of claim 18, wherein the memory further comprises programming instructions that cause the processing unit to enable the graphics processing circuit to receive incoming data via the local bus when at least one address identifies the graphics processing circuit and when the associated command is for inputting data.

21. The arbitrator of claim 18, wherein the memory further comprises programming instructions that cause the processing unit to provide the audio processing circuit access to

the local bus when the at least one address identifies the audio processing circuit and the associated command is for outputting data.

22. The arbitrator of claim 18, wherein the memory further comprises programming instructions that cause the processing unit to provide the graphics processing circuit access to the local bus when the at least one address identifies the graphics processing circuit and the associated command is for outputting data.

23. The arbitrator of claim 18, wherein the at least one address comprises a plurality of addresses, and wherein the memory further comprises programming instructions that cause the processing unit to intermix the audio processing circuit's access to the local bus with the graphics processing circuit's access to the local bus based on the plurality of addresses and the associated command.

METHOD AND APPARATUS OF VIDEO GRAPHICS AND AUDIO PROCESSING

Abstract of the Disclosure

A method and apparatus for combining video graphics processing and audio processing onto the same single chip and/or printed circuit board includes a graphics processing circuit, an audio processing circuit, a local bus, and a bus arbitrator. The local bus couples both the graphics processing circuit and audio processing circuit to the system bus such that each of the circuits may transceive data with the system bus. The bus arbitrator arbitrates access to the local bus between the graphics processing circuit and audio processing circuit. Such arbitration is based on incoming data, which is interpreted and, based on the interpretation, the bus arbitrator routes the incoming data to either the graphics processing circuit or the audio processing circuit. In addition, the bus arbitrator arbitrates outputting data from the graphics processing circuit and the audio processing circuit based on commands received from the CPU.

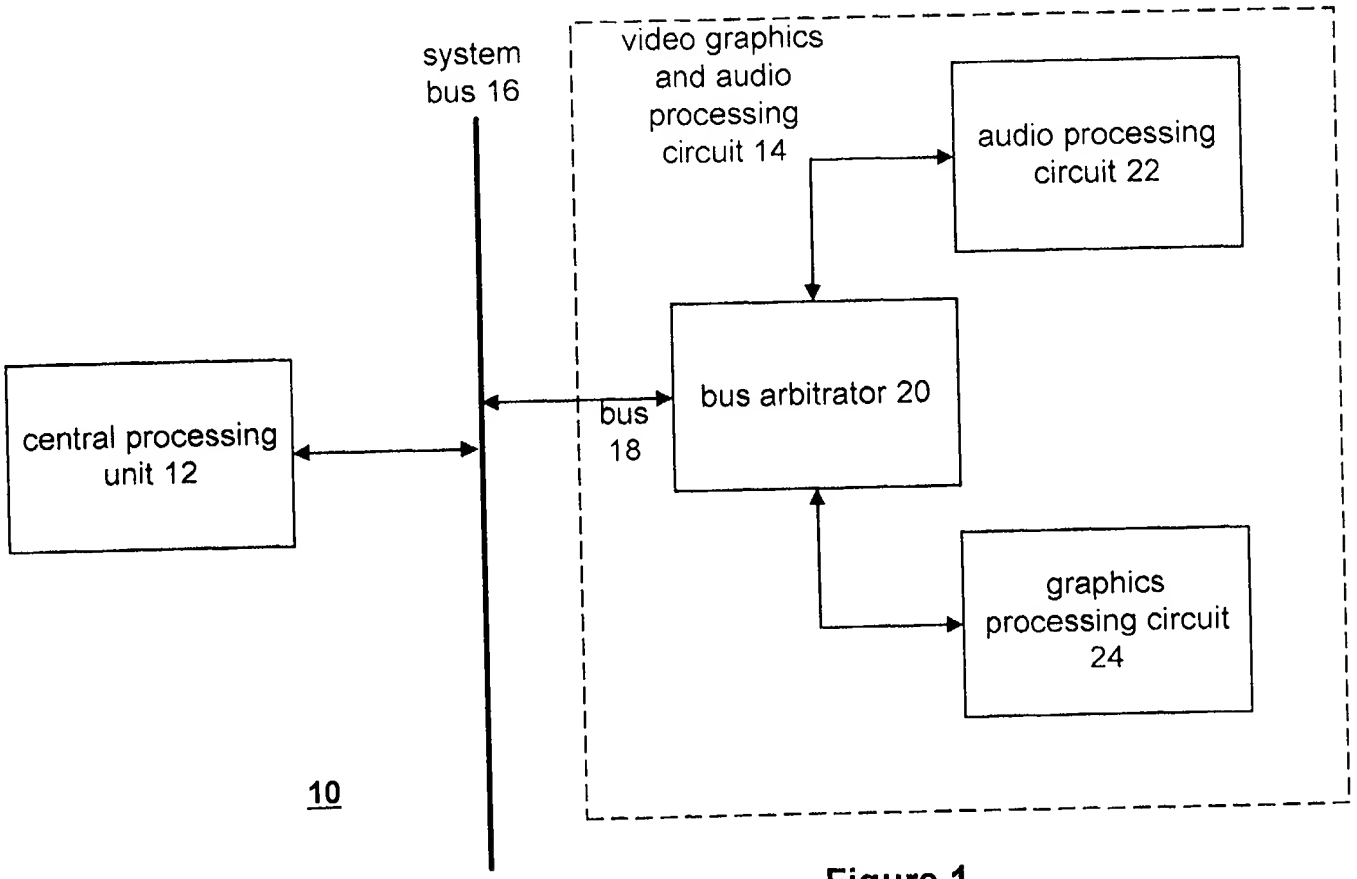

system
bus 16
video graphics
and audio
processing
circuit 14
audio processing
circuit 22
bus arbitrator 20
bus
18
central processing
unit 12
graphics
processing circuit
24
10

Figure 1

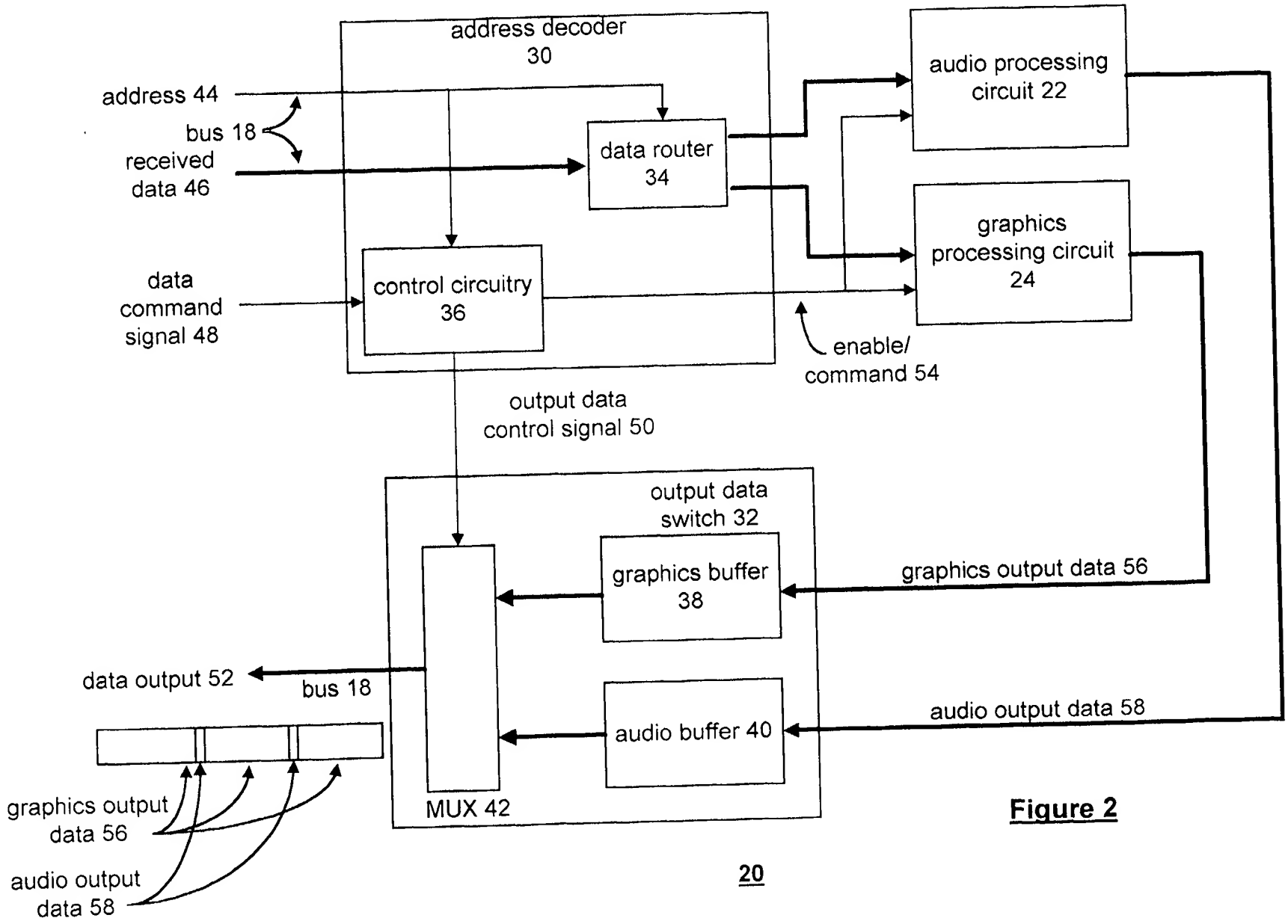
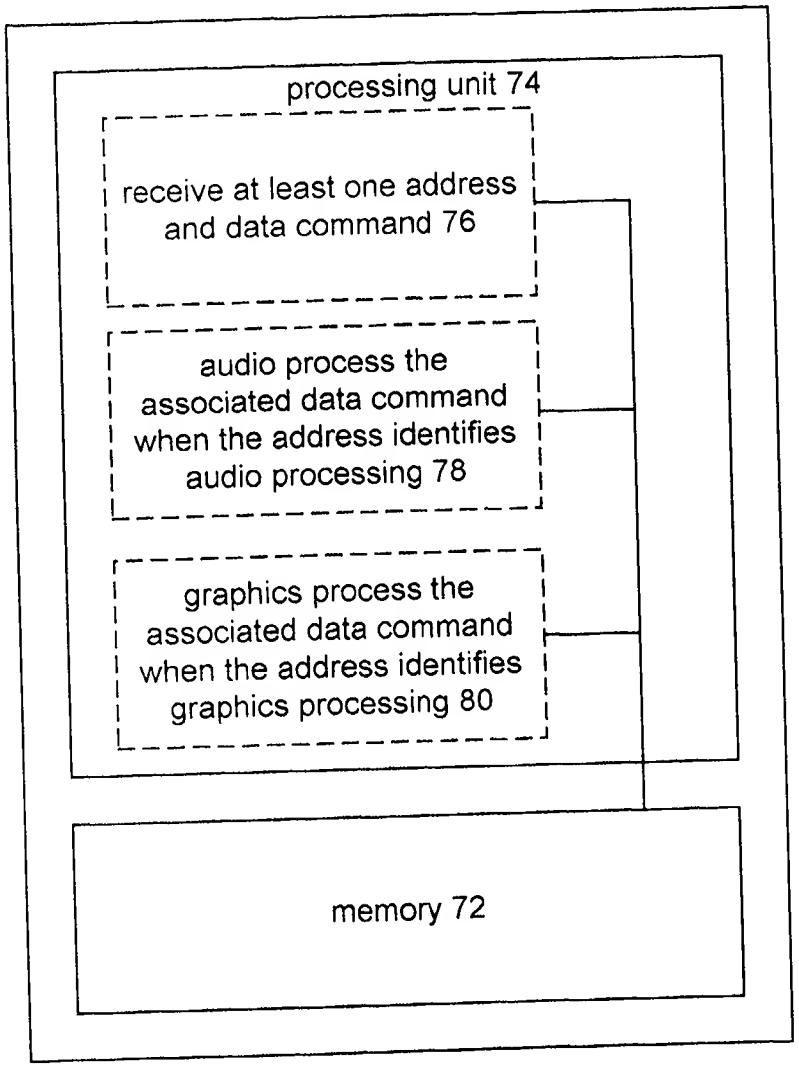
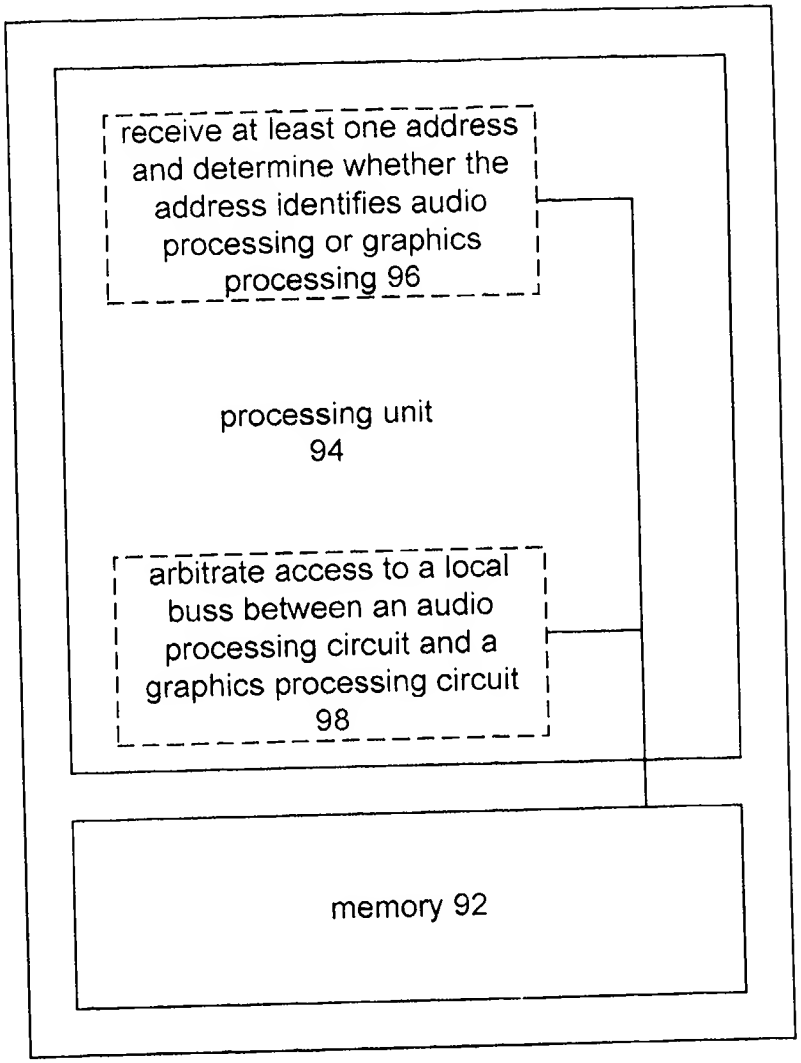

address decoder
30
address 44
bus 18
received
data 46
data router
34
audio processing
circuit 22
graphics
processing circuit
24
data
command
signal 48
control circuitry
36
enable/
command 54
output data
control signal 50
output data
switch 32
graphics buffer
38
graphics output data 56
data output 52
bus 18
audio buffer 40
audio output data 58
MUX 42
graphics output
data 56
audio output
data 58
20

Figure 2



video graphics and audio processing circuit 70

Figure 3



arbitrator 90

Figure 4

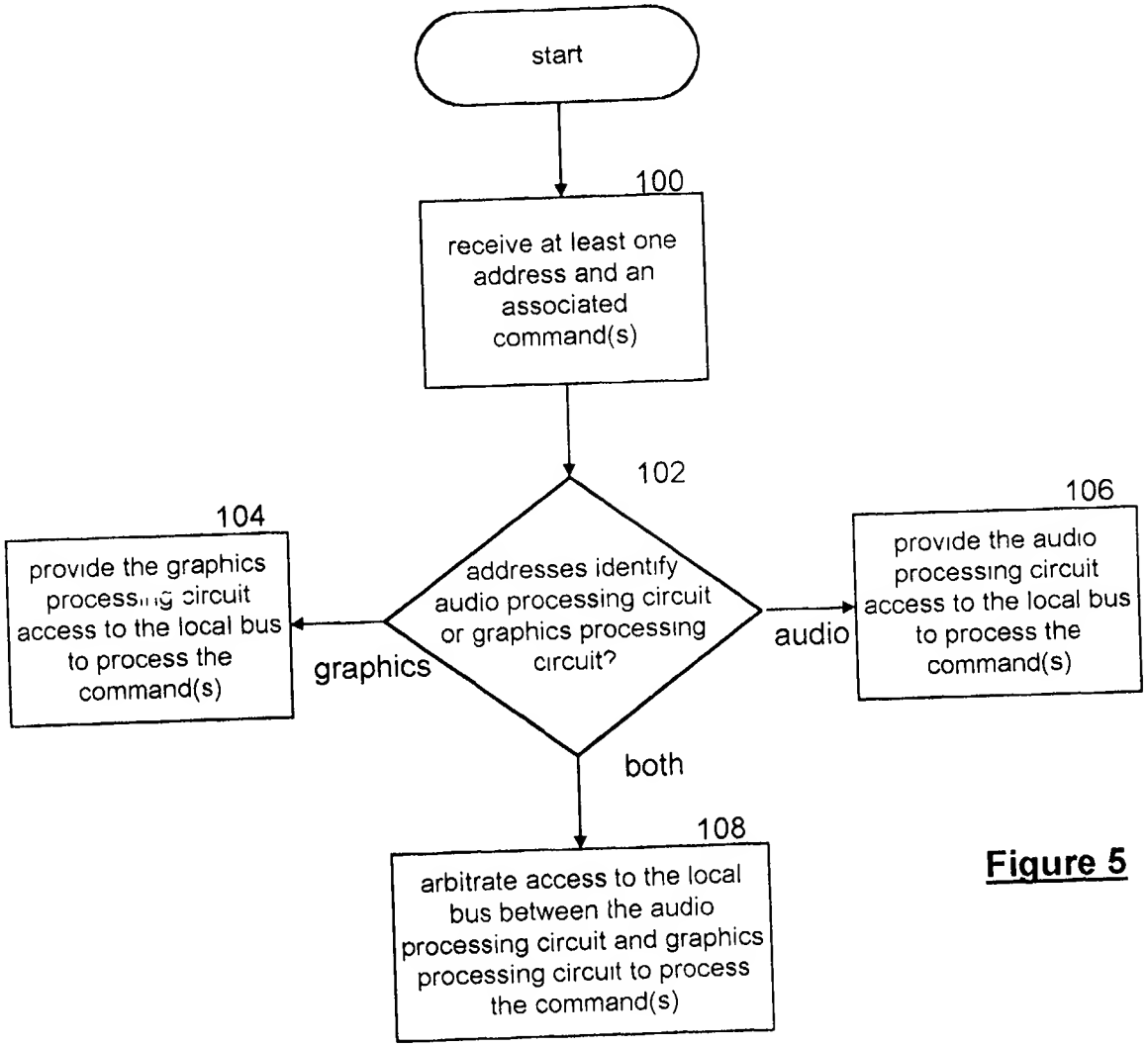

start
100
receive at least one address and an associated command(s)
102
addresses identify audio processing circuit or graphics processing circuit?
graphics
audio
both
104
provide the graphics processing circuit access to the local bus to process the command(s)
106
provide the audio processing circuit access to the local bus to process the command(s)
108
arbitrate access to the local bus between the audio processing circuit and graphics processing circuit to process the command(s)

Figure 5

PATENT APPLICATION
Docket No . 0100 01142

DECLARATION AND POWER OF ATTORNEY
Pursuant to 37 C F R 1 63 and 1 67

As a below named inventor. I hereby declare that

My residence, post office address and citizenship are as stated below next to my name, and

I believe that I am the original and first sole inventor of the subject matter of a patent application entitled: METHOD AND APPARATUS OF VIDEO GRAPHICS AND AUDIO PROCESSING The specification for the patent application (check one)

☒	is attached hereto
☐	was filed on as Application Serial No and was amended on (if applicable)
☐	was filed as PCT International Application No PCT/ on and was amended on (if applicable)
☐	was filed on as Application Serial No and was issued a Notice of Allowance on

I hereby state that I have reviewed and understood the contents of the above identified patent application, including the claims as amended by any amendment referred to above or as allowed as indicated above

I acknowledge the duty to disclose all information known to me to be material to the patentability of this patent application as defined in 37 C F.R. Section 1 56 for the pendency of the application If this is a continuation-in-part (CIP) application, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U S C Section 112, I acknowledge the duty to disclose to the Office all information known to me to be material to patentability of the application as defined in 37 C F R Section 1 56 which became available between the filing date of the prior application and the national or PCT international filing date of this CIP application

I hereby claim foreign priority benefits under 35 U S C Sections 119 and 365 of any foreign application(s) for patent(s) or inventor's certificate(s) listed below I have also identified below any foreign application(s) for patent(s) or inventor's certificate(s) filed by me or my assignee which
disclose the subject matter claimed in this patent application, and
have a filing date that is either
(1) before the filing date of the application on which my priority is claimed, or,
(2) before the filing date of this application when no priority is claimed

Prior Foreign Patents

priority claimed	Number	Country	Mo/Day/Yr Filed	Date First Laid Open or Published	Date Granted or Patented
☐					
☐					
☐					

I hereby claim the benefit under 35 U S C Sections 120 and 365 of any United States application(s) listed below and PCT international application(s) listed below

Prior U.S. or PCT Applications

Application No.	Mo/Day/Yr Filed	Status

I hereby Timothy W Markison, Registration No 33,534, Christopher J Reckamp, Registration No 34,414, Robert M. McDermott, Registration No. _____, Paul Anderson, Patent Agent, Registration No. ___ all attorneys (or agents) with the firm of MARKISON & RECKAMP, P.C having its principal place of business at 899 Skokie Boulevard- Suite 332, Northbrook Illinois 60062, and Sally Daub, Patent Agent, Registration No 41478 of ATI Technologies, Inc as my attorneys. with full power of substitution and revocation, to prosecute this patent application and to transact all business in the United States Patent and Trademark Office connected therewith, and to file and prosecute any international patent applications filed thereon before any international authorities under the Patent Cooperation Treaty, and I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct them in writing to the contrary

Please address all correspondence and direct all telephone calls to
MARKISON & RECKAMP, P C.
P O Box 677
Northbrook, Illinois 60065
Phone (847) 564-9050

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this patent application or any patent issued thereon

Inventor(s)

Full Name Raymond Li Citizenship: Canadian

Signature Raymond Li Date 20th March 98

Street Address 145 Featherstone Ave

City Markham State or Province Ontario Zip or Postal Code L3S 3M7 Country Canada

Full Name Citizenship:

Signature _____ Date _____

Street Address

City State or Province Zip or Postal Code Country

Full Name Citizenship:

Signature _____ Date _____

Street Address

City State or Province Zip or Postal Code Country

Full Name Citizenship:

Signature _____ Date _____

Street Address

City State or Province Zip or Postal Code Country

Full Name Citizenship:

Signature _____ Date _____

Street Address

City State or Province Zip or Postal Code Country